Multi-Channel Transcutaneous Cortical Stimulation System

Contract # N01-NS-7-2365

Progress Report #8

for the contract period 2/1/99 – 4/30/99

Illinois Institute of Technology

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Introduction

The goal of this project is the design, fabrication, and testing of a ***Multi-Channel Transcutaneous Cortical Stimulation System*** to be used in a prototype artificial vision system**.** During the past 25 years, the development of a neuroprosthesis that could be used to restore visual sensory functions has been an important goal of the Neural Prosthesis Program (NPP) of the National Institute of Disorders and Stroke, National Institutes of Health. Demonstrations of the feasibility of a visual prosthesis have reached the stage in which the NPP is highly motivated to initiate the development of a fully implantable cortical stimulation system which could be used to provide inputs and computer control for hundreds, to over one thousand, implanted cortical electrodes. This project uses the combined capability four organizations, the Illinois Institute of Technology, BioElectric Inc., Cross Technology, and the A.E. Mann Foundation to accomplish this challenging task.

This is the eighth progress report for this project. In this report we describe our progress on defining fabrication methods for the hermetic seals, fundamental tests of the glass to ceramic seals and our progress on the ASIC designs.

Progress on Design of the Implant Package

In our seventh progress report we reported that we had defined tooling patterns for alignment of the Macor substrates at Electrofilms and IIT. These tooling patterns are essential so that the metal deposition, on the ceramic, done at Electrofilms, can be aligned with the numerical-controlled milling operation of the substrates at IIT. During the this quarter we met with Electrofilms in order to more precisely define the fabrication steps involved in preparing larger numbers of ceramic package samples.

In addition, we felt the need to perform comprehensive analytical tests on the glass to ceramic seals. These will include bond-strength tests, finite element analysis of residual stress, wetting tests, and chemical stability tests.

Seal Fabrication

By way of review, in Figure 1, we show the location of one of the glass-to-ceramic seals between ceramic layer #2 and ceramic layer #3. The seal is formed by depositing the glass, in the green state, on layer #2 via a syringe controlled by the X-Y-Z table. The green glass is dried at 100ºC – 150ºC in a convection oven. Layers #2 and #3 are pressed together, then fired in a furnace using a ramped temperature profile at a maximum of 380ºC.

The glass must seal against the ceramic, as well as the gold interconnection feedthroughs. We have some concern about the adhesion of the glass to the gold. In discussing this potential problem with Electrofilms, we decided upon a strategy to eliminate the potential problem, rather than simply testing to understand its magnitude.

The metal feedthroughs will be fabricated by depositing a base layer of tantalum nitride, followed by a titanium-tungsten adhesion layer, followed by the final gold top layer. The gold and titanium-tungsten will then be etched away in the region of the glass seal. This concept is

shown in Figure 2, below. In Figure 2, the blue areas depict the location of the tantalum nitride conductors. This approach has another electrical benefit: the tantalum nitride conductor, within the seal region, will have an electrical resistance of about 30-70 ohms. This resistance will be in series with the electrode outputs, and provides a mechanism of protection against electrostatic discharge damage. We intend to start testing seals that use this structure within the next two months.

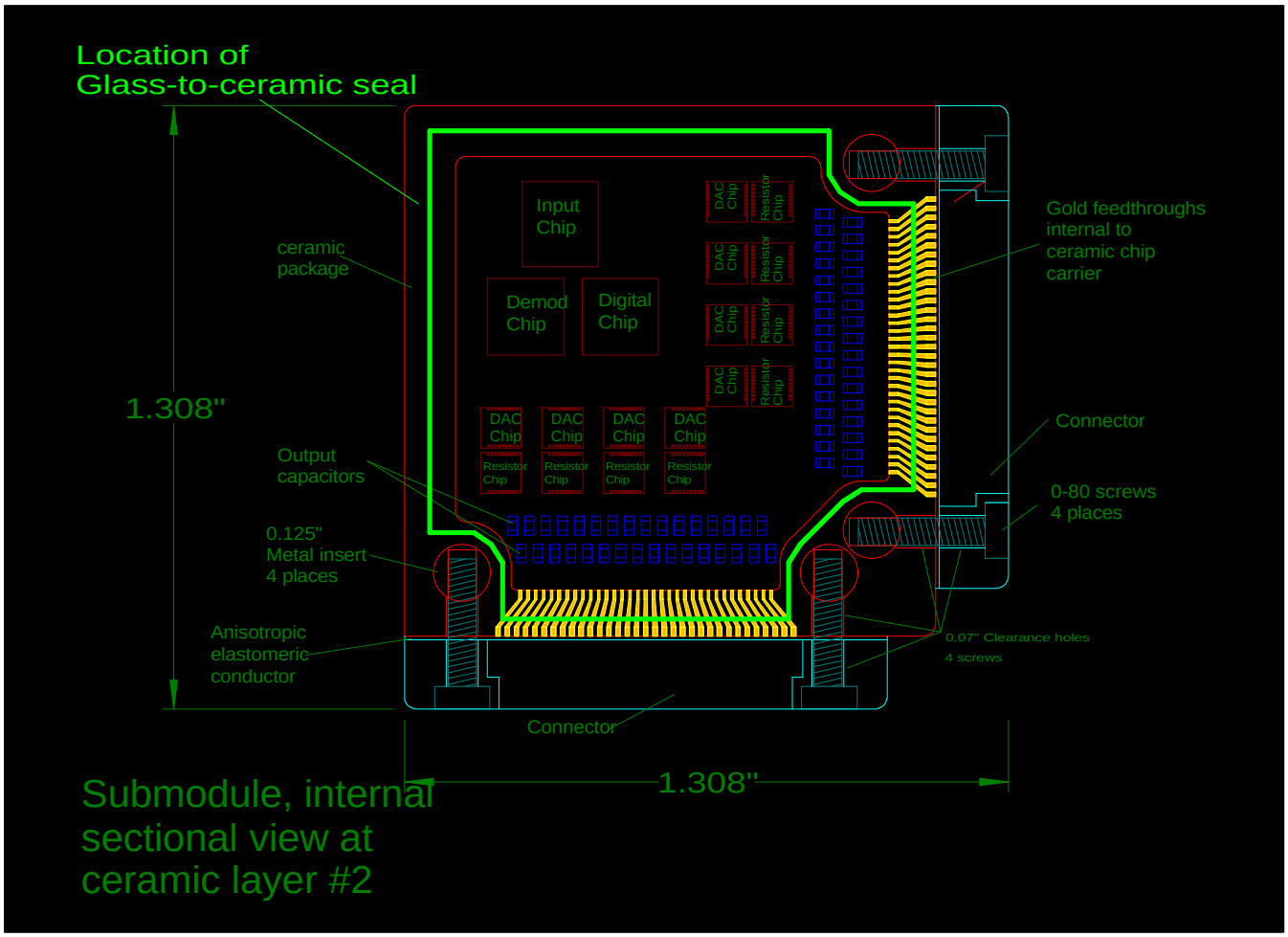

Figure 1 – Submodule section at layer #2 showing location of the glass seal.

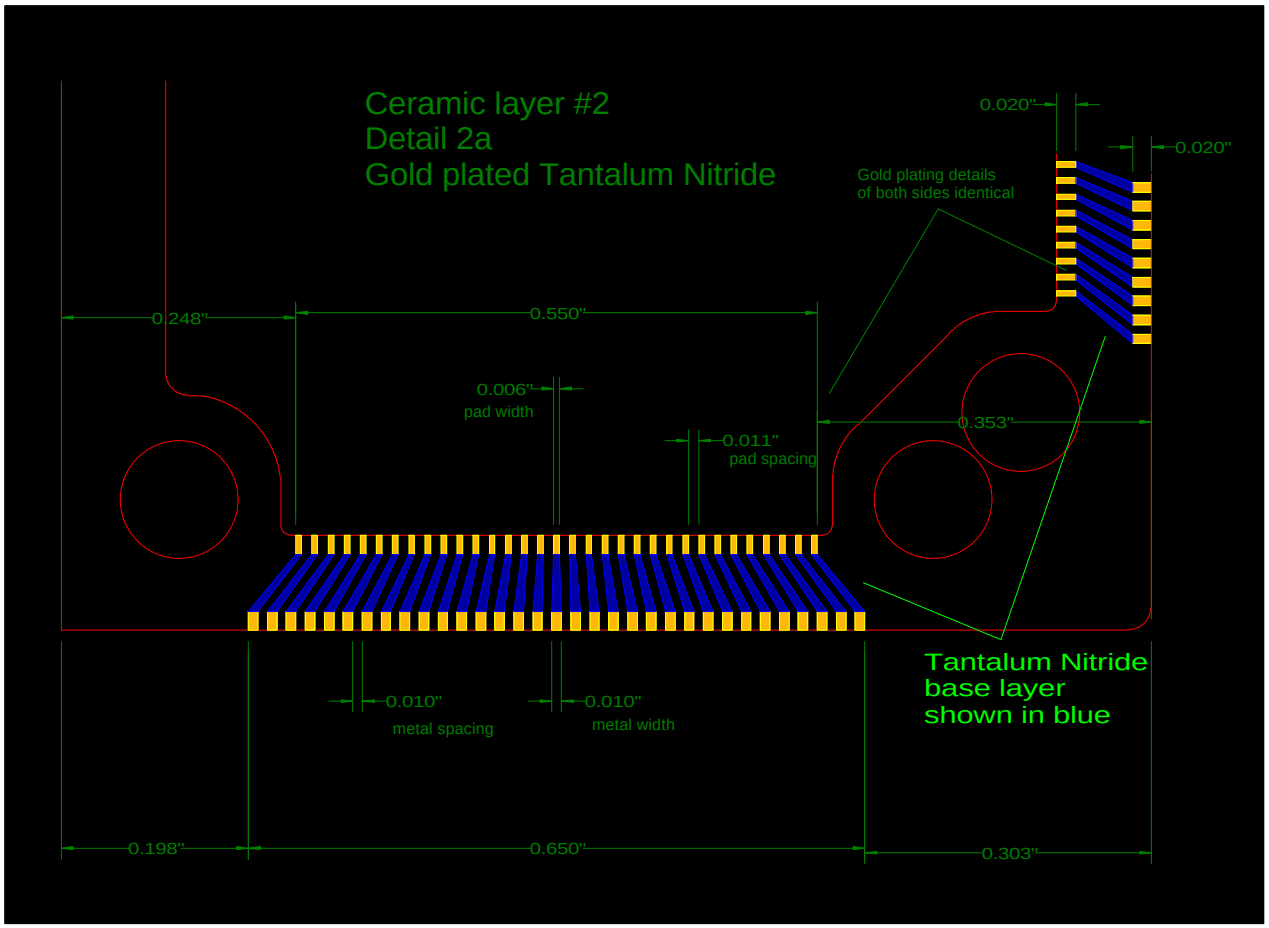

Figure 2 – Detail of the electrical feedthroughs showing the location of the tantalum nitride

Analytical Tests on the Glass Seals

Presently we are defining a range of analytical tests to be performed on the glass seals and the seal design. Candidate tests are described below.

1. Mechanical properties:
We will determine whether the binding strength is a function of firing temperature. Samples made by using different maximum firing temperatures will be tested for tensile strength on an INSTRON test machine.

(a). For sealing glass B-10041 (vitreous): Softening point: ~343°C,
Firing Temperature: ~370°C.
Seven different firing temperatures will be tested: 330, 340, 350, 360, 370, 380, 390 °C.

(b). For sealing glass B-10042 (crystalline): Softening point: ~336°C,
Firing Temperature: ~370-400°C.

Nine different sintering temperatures will be tested: 320, 330, 340, 350,360, 370, 380, 390, and 400°C.

The details of this tensile test such as the design of shape of the samples will be developed to fit the specific seal material. After each tensile test, the fracture surface should be examined, and photographs should be taken for records of the microstructure. These tests will be designed during the next quarter.

To obtain better understanding of the seal, the microstructure of the seal materials and the interface between glass seal and ceramic substrate should be studied thoroughly. Scanning electron microscope (SEM) may be applied.

2. Residual Stress Analysis by using Finite Element Method.

During the heat treatment process, the difference between the thermal expansion coefficient of glass seal and ceramic substrates will cause a certain level of residual stress. Glass has a low thermal conductivity, which can cause thermal gradients in the sealed substrates. Quantitative analysis is needed to ensure the two coefficients are adequately matched.

The calculation should include two kinds of glass seal materials: B10041 and B10042. For each material, the residual stress analysis simulation should be done for both minimum and maximum firing temperatures.

3. Wetting Angle Measurement

To measure the wetting angle accurately, rectangular shaped glass seals will be prepared. After mounting, the sample wetting angle will be measured under a microscope.

4. Chemical stability of the glass seal

Considering of the composition of the low firing temperature glass seal material and the application environment, the chemical stability of all materials including both the seal material and drying vehicles must be studied thoroughly. The chemical durability of each glass seal can be judged from its dissolution rate in distilled water at 100°C for a prolonged period of time. The dissolution rate (DR) was defined as the weight loss per minute from 1 cm^2 of surface. Similar testing will be performed in physiologic fluids.

Progress on the design and fabrication of the submodule ASICs.

During the past quarter we have tested a revised the BLOCK ASIC BLOCK3. We have also made progress on designing a microcontroller, connected to a PC for testing, control, and laboratory use of the 8-channel BLOCK chips.

Testing of BLOCK3

During the testing of BLOCK2, we had observed some mismatch between identically designed DACs on the same die. In evaluating BLOCK2, we had found an improvement, over earlier designs, in the anodic-to-cathodic matching. For some DACs the match was as close as 2%. However, for other DACs the mismatch was larger, up to 15%. In order to achieve a wide compliance voltage range, we used a unique regulation of the current mirror voltages, as described in our earlier reports. We had determined that variations in the offset voltage of the voltage regulators was responsible for the DAC-to-DAC variations.

We believed that these variations were caused by lithographic differences between identical DAC stages on the same chip. We were impressed and surprised by our measurements that showed significant differences between identically-sized transistors, that we nearly adjacent to each other on the same die. Therefore, we had previously reported that we had performed a Monte Carlo variation in the length and width of our transistor models in our SPICE computer simulations. Using this method, we concluded that a size increase of approximately six times was required for critical DAC transistors. We had modified the DAC cells of BLOCK2 and submitted a new design, BLOCK3, for fabrication. By way of review, the size change in the regulator and output transistors of BLOCK3, compared to BLOCK2 can be seen in Figure 3, below. Note the use of much larger transistors for the ones that need to be critically matched.

In tesing of BLOCK3, our earlier hypothesis was confirmed. The DAC-to-DAC matching, within a single die was excellent, on the order of 1%. The tracking between the lower and higher order bit groups was similar. Compliance voltages were measured of approximately 0.2 volts to 10 volts for the current sources, and 0.2 volts to 9.6 volts for the current sinks. The current sinks show increased current at the higher voltages due to residual impact ionization currents that are not corrected by the output stage cascode. However, we feel that the matching between source and sink, the DAC-to-DAC matching, and the compliance voltage range is more than adequate for visual prosthesis application.

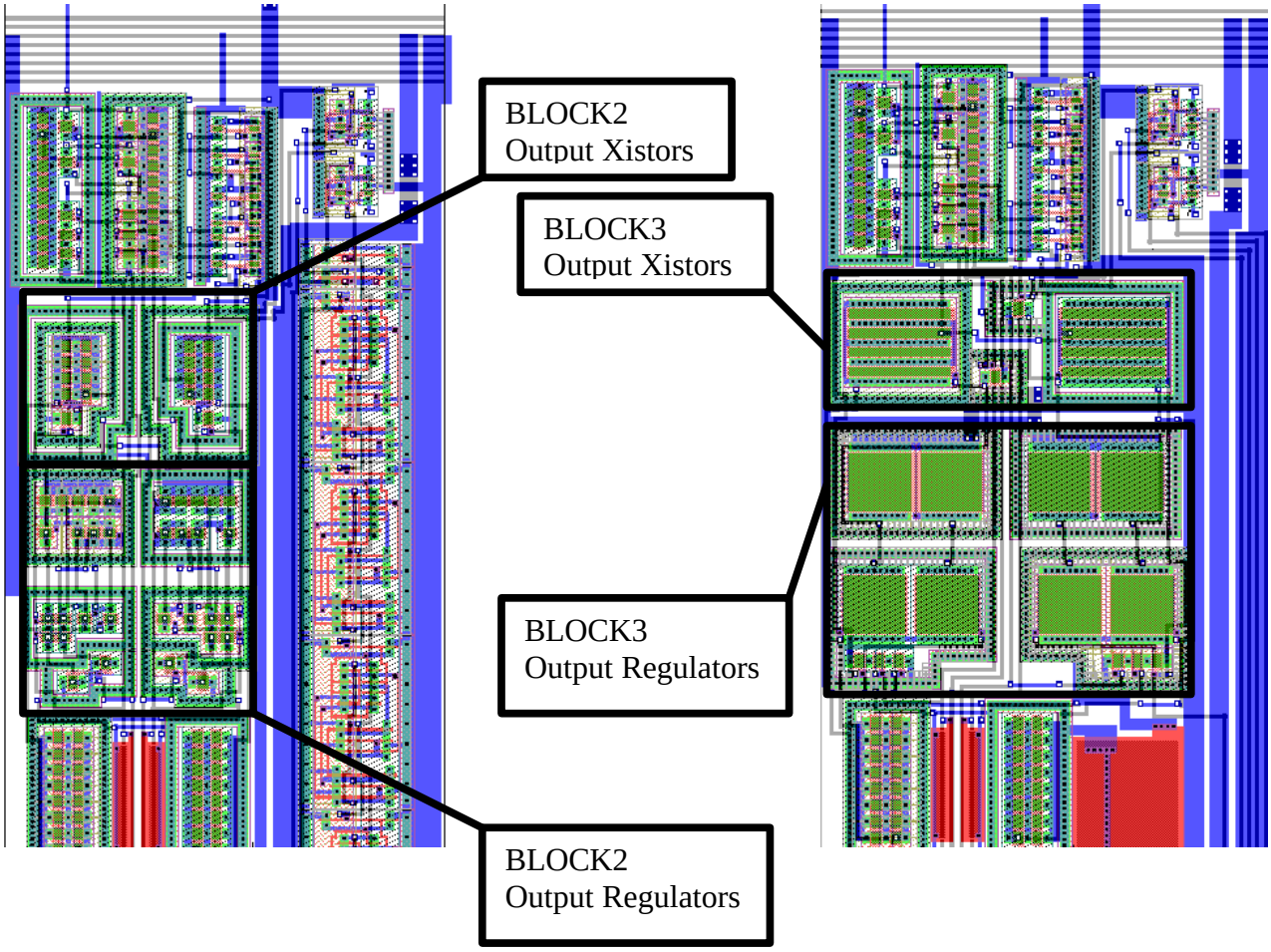

Figure 3 – Comparison between BLOCK2 and BLOCK3 output transistors

To test the BLOCK chips we have, to date, used a simple 80C51 processor. During this quarter we made progress on the implmenation of a more extensive PC-based controller. This controller is intended to be the first step in the laboratory use of the BLOCK chips. The format of the data communication with the BLOCK chips is identical to that which we will use when the implant state machine is completed. This controller will not only permit bench testing of the BLOCK chips, but would alsobe available for driving implanted electrodes, at NIH.

We now intend to proceed with the design of the implant state machine. The state machine will decode the digital data sent over the inductive transcutaneous link, and create the necessary digital data streams to control each of the BLOCK chips.

To facilitate this process we have adapted the SYNOPSIS VHDL simulation and design tool to be compatible with the TANNER layout tools. SYNPOSIS is used in our VHDL

workstation design laboratory for design and simulation of logic networks. Unfortunately it does not produce an output file that is compatible with the TANNER tools, our ASIC layout editor. In this quarter we have written a file translator that adapts the output format of the SYNOPSIS tool with the TANNER tools. The TANNER tools will then be used to perform an automatic place and route. The translator has been tested and is ready for use. In the next quarter we will begin design of the state machine.